(c) a task switching circuit for controlling the execution of tasks in a sequence determined by the task priority selection circuit.

5. The interrupt and task change processing circuit of claim 4 wherein said task priority selection circuit includes a variable rate task priority incrementing circuit for varying an assigned priority of a task such that said priority increases with time, whereby its execution is caused by to occur within a predetermined period of time.

6. The interrupt and task change processing circuit of claim 4 wherein the task enable circuit includes a task linking circuit for linking together a plurality of tasks in a predetermined order.

7. The interrupt and task change processing circuit of claim 4 wherein the task enable circuit includes a timer for generating a task interrupt signal after a predetermined period of time.

8. The interrupt and task change processing circuit of claim 4 wherein the task switching circuit includes a trace enable circuit for recording register states on selected registers during a preselected clock cycle.

9. The interrupt and task change processing circuit of claim 4 wherein the task switching circuit includes a zero overhead multiplexing circuit for storing a later task in a first set of latches during a first clock cycle while simultaneously switching a